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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,956	12/20/2001	Benjamin Tang	35706.5700/65	5412

34398 7590 04/18/2006

PRIMARION, INC.
PRIMARION LEGAL DEPT.
3650 E. WIER AVENUE
PHOENIX, AZ 85040

EXAMINER	
EL HADY, NABIL M	

ART UNIT	PAPER NUMBER
2152	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,956	TANG ET AL.	
	Examiner	Art Unit	
	Nabil M. El-Hady	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-35 are pending in this application.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-35 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 20-29 of copending Application No. 10/029,709, hereinafter "709". Although the conflicting claims are not identical, they are not patentably distinct from each other because both "709" and the instant application disclose similar components of a PLL/DLL dual loop data serializer.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

16are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following words or phrases are not clearly understood, rendering corresponding claims vague or indefinite:

a) "PISO", claim 1, line 12, and claim 10, line 12, is not defined.

b) "VOC", claim 10, line 4, is not defined.

B. The following lacks antecedent basis:

a) "said fill level", claim 10, line 7.

b) "said pre-filtered signal input", claim 10, line 10.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted prior Art, hereinafter "AAPA" in view of Kaylani et al. (WO 00/46949), hereinafter "Kaylani".

7. Kaylani is cited by the applicant in IDS paper.

8. As to claim 1, AAPA discloses a PLL/DLL dual loop data synchronization system comprising a phase lock loop (PLL) including, a phase frequency detector (PFD) receiving a local clock, a voltage controlled oscillator (VCO), a loop filter coupled to said PFD and to said VCO, said loop filter configured to suppress VCO phase noise, and a phase shifter coupled to said VCO and configured in a feedback loop with said PFD; a delayed lock loop (DLL) having a digital loop filter coupled to a phase detector and to said phase shifter of said PLL (Fig. 4).

9. AAPA does not disclose a FIFO register receiving data input and outputting a signal to said phase detector. Kaylani, on the other hand, discloses a FIFO register receiving data input and outputting a signal to said phase detector (page 1, lines 30-32). It would have been obvious to one skilled in the art at the time of the invention to modify the teachings of AAPA with that of Kaylani and using a FIFO register to receive data input and output a signal to the phase detector because a signal representative of the state of the FIFO would be used to enhance the control of the selection of the phase shifted output signal (see, Kaylani, page 1, lines 30-32).

10. AAPA does not disclose using the data synchronization system as a serializer. However, it would have been obvious to one skilled in the art at the time of the invention that using the data synchronization system of AAPA as a serializer means that the input data is parallel data and a PISO serializer would be used when serialized data is expected as output data.

11. As to claim 10, the claim is rejected for the same reasons as claim 1 above. In addition, AAPA discloses detecting a local reference at a PDF of a PLL (Fig. 5). Kaylani, however, filter a signal representative of fill level of the FIFO (state of the FIFO, page 1, line 31).

12. As to claims 17, 23 and 29, the claims are rejected for the same reasons as claim 1 above. In addition, AAPA discloses a plesiochronous data retimer comprising a digital delay lock loop (DDLL) receiving an input data to be retimed and configured to recover a clock of said input data (Fig. 4). It would have been obvious to one skilled in the art at the time of the invention that using the data synchronization system of AAPA as a retimer with serial input data would require desirlizar (SIPO) to reference the data to the clock, followed by a serializer (PISO), and hence, SIPO, FIFO, and PISO for transmitting the retimed data.

13. As to claim 2, it would have been obvious to one skilled in the art at the time of the invention that the DLL is embedded in said PLL or separate from PLL is a design choice.

14. As to claim 3, Kaylani discloses said PLL locks to said signal from said FIFO to said phase detector (page 1, lines 30-35).

15. As to claims 4 and 12, AAPA discloses said loop filter of said PLL comprises a wideband filter (spec., [0009]).

16. As to claims 5 and 13, AAPA discloses said loop filter of said DLL comprises a narrowband filter (spec., [0011]).

17. As to claim 6, Kaylani discloses said signal to said phase detector comprises a FIFO fill level indicator (state of the FIFO, page 1, line 31).

18. As to claims 7, 14, 25, and 33, Kaylani discloses said phase detector is configured to translate said FIFO fill level into a digital value (Fig. 5).

19. As to claims 8, 16, and 35 AAPA discloses the data stabilizer for use in a plesiochronous system (Figs. 2 and 3).

20. As to claim 9, the claim is rejected for the same reasons as claims 17, 23, and 29 above.

21. As to claims 11 and 30, AAPA discloses the step of outputting a synthesized clock (Fig. 4).

22. As to claims 15 and 34, the claims are rejected for the same reasons as claim 10 above. In addition, AAPA discloses said translating step comprises a phase detector in said DLL (Fig. 4).

23. As to claim 18, the claim is rejected for the same reasons as claim 17 above. In addition, AAPA discloses said DDLL comprises a phase detector and a digital loop filter (Fig. 4).

24. As to claim 19, AAPA discloses said loop filter of said DDLL comprises a wide bandwidth (spec., [00011]).

25. As to claim 20, the claim is rejected for the same reasons as claim 17 above. In addition, AAPA discloses said serializer comprises a loop filter within said PLL (Fig. 4).

26. As to claim 21, the claim is rejected for the same reasons as claim 17 above. In addition, AAPA discloses said serializer comprises a dual bandwidth (spec., [0011].

27. As to claim 22, the claim is rejected for the same reasons as claim 17 above. In addition, AAPA discloses said DLL loop filter comprises a narrow bandwidth and said PLL loop filter comprises a wide bandwidth (spec., [0009], [0011]).

28. As to claims 24 and 31, the claims are rejected for the same reasons as claim 23 above. In addition, AAPA discloses said synthesizing step comprises phase locking said VCO to a local reference (Fig. 4).

29. As to claim 26, the claim is rejected for the same reasons as claim 23 above. In addition, Kaylani discloses said writing step and said reading step comprise a write clock of said FIFO and a read clock of said FIFO, respectively (Fig. 5).

30. As to claim 27, the claim is rejected for the same reasons as claim 23 above. In addition, Kaylani discloses phase locking said write and read clocks of said FIFO in said DLL (Fig. 5).

31. As to claim 28, the claim is rejected for the same reasons as claim 23 above. In addition, Kaylani and AAPA disclose locking said VCO output to said FIFO write clock (Figs.3 and 5), and AAPA (Fig. 4.).

32. As to claim 32, AAPA discloses said PLL filtering step comprises a wide bandwidth filtering (spec., [0009]).

33. Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nabil M. El-Hady whose telephone number is (571) 272-3963. The examiner can normally be reached on 9:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on (571) 272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 14, 2006

Nabil El-Hady, Ph.D, M.B.A.
Primary Examiner
Art Unit 2152